A Quantum Computing Simulator
Milestone Report

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1 Revised Schedule

Weeks	Target	Time Period
Week 1	Project planning	2026-03-23 - 2026-03-29
Week 2	Investigate the openqasmtools and implement the the conversion from QASM to the internal representation. CPU within-gates implementation	2026-03-30 - 2026-04-05
Week 3	CPU OpenMP implementation and preliminary performance test. Initial GPU within-gate implementation	2026-04-06 - 2026-04-12
Week 4-1	Merge and test the GPU within gate implementation, as well as small scale performance comparison with CPU.	2026-04-13 - 2026-04-16
Week 4-2	CPU+OpenMP/GPU across-gate implementation	2026-04-17 - 2026-04-19
Week 5-1	Select a set of representative benchmarking programs for final performance test.	2026-04-20 - 2026-04-21
Week 5-2	Carry out performance test and result analysis	2026-04-21 - 2026-04-23
Week 5-3	Sketch and finalize the poster and the report	2026-04-23 - 2026-04-26

2 Work completed

We have implemented the conversion from OpenQASM 2.0 to our internal representation of a quantum circuit and implemented the reference CPU and OpenMP kernels for simulation of the circuits.

We have implemented the beta version of CUDA within-/across- gate with correctness ensured. However, we have not merged the feature into the main branch. Current implementation indicates that we have better performance under larger qubits scenarios in comparison to CPU version.

3 Poster Sessions

We intend to present the performance graph and data of the speedups on varying benchmarking programs, as well as the visualized quantum circuits to show the characteristics of the programs.

4 Preliminary Results

We currently have small scale performance test results on CPU and OpenMP implementation. On some benchmarking cases (e.g., `QASMBench/medium/bigadder_n18` and `QASMBench/medium/dnn_n16`), we found that the performance is highly program-dependent. On the programs with more qubits (larger statevector) and less gates, we reached near-linear speedup. On `QASMBench/medium/bigadder_n18`, we reached $\tilde{3}$.8x on 4 threads and $\tilde{7}$x speedup on 8 threads. However, on programs with less qubits but significantly more gates, the speedup is lower. On `QASMBench/medium/dnn_n16`, we only achieved $\tilde{4}$x speedup on 8 threads. This could result from larger portion of the serialized part of program according to Amdahl's law.

5 Concerning Issues

We need to choose some representative benchmark programs to demonstrate the performance of our implementations.

We currently have an initial idea of implementing the across-gate parallelization method. However, we still need to verify whether it would work.

6 Other Revised Design Decisions

We decide not to implement the full measurement/probabilistic-sampling in the simulator, but to focust on the optimization of the simulation process of the cirsuits. This is because the main scope of this our project is accelerating the statevector simulation of quantum circuits.